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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,668	03/17/2004	Terunao Hanaoka	81754.0118	2671

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HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
DOAN, THERESA T	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 07/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/802,668	HANAOKA, TERUNAO	
	Examiner	Art Unit	
	Theresa T. Doan	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *7-10,14,17 and 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,11-13,15,16,18 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/07/05& 03/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The prior art documents submitted by applicant in the Information Disclosure Statement filed on 03/07/05 and 03/17/04, have all been considered and made of record (note the attached copy of form PTO-1449).

Drawings

2. The drawings, filed on 03/17/04, are accepted.

Election/Restrictions

3. Applicant's election of claims 1-6,11-13, 15-16 and 18-19 in the reply filed on 06/10/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-6, 11-13, 15-16 and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamaguchi (U.S. Pub. 2004/0166660).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding claim 1, Yamaguchi (Fig. 2) discloses a semiconductor device, comprising:

a semiconductor substrate 10 including an integrated circuit 12 (paragraph [0077]) and an electrode (14,16) (paragraph [0078]);

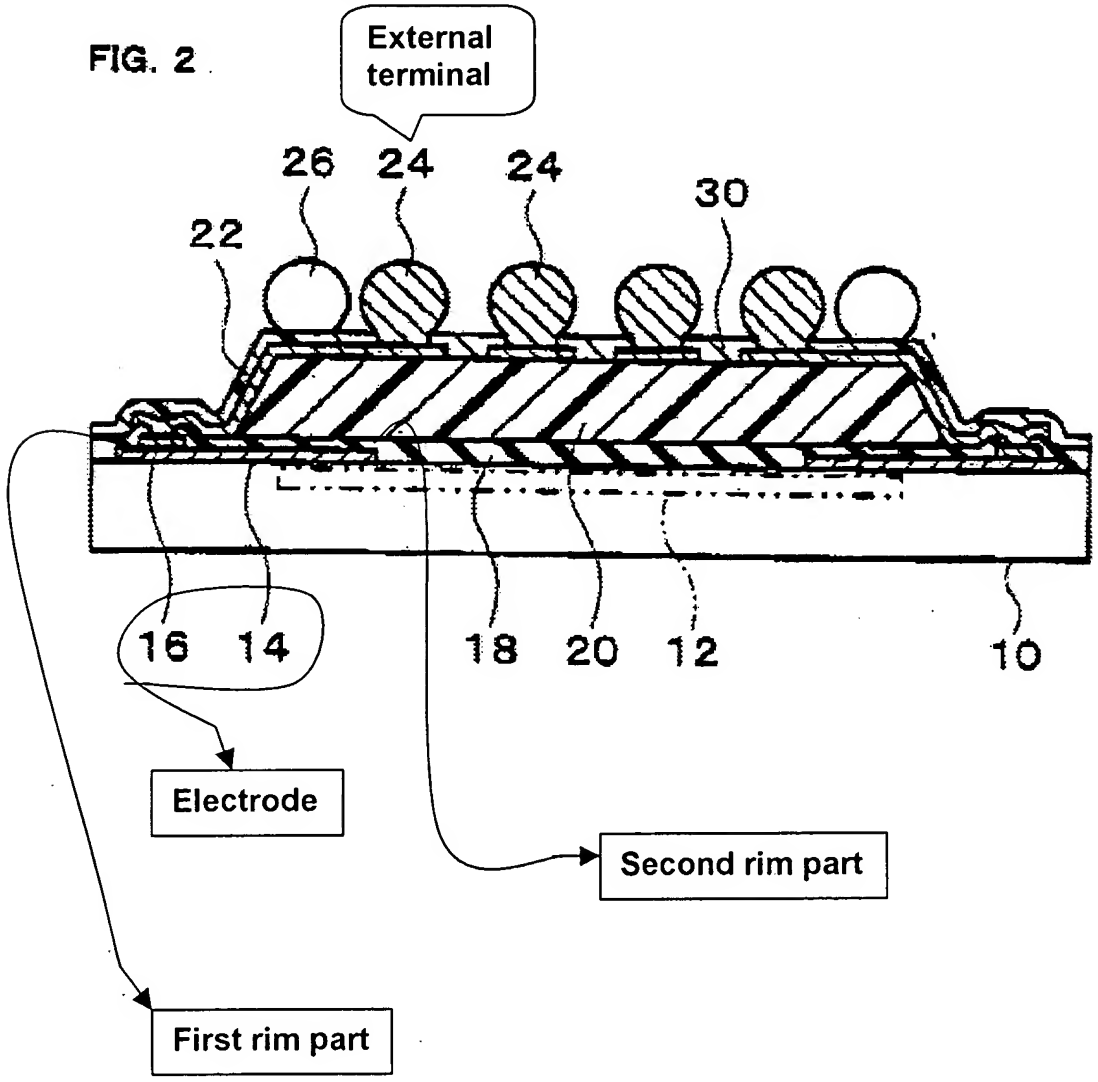
a resin layer 20 provided on a side of the semiconductor substrate 10 where the electrode (14,16) is formed (paragraph [0080]); and

a wiring layer 22 formed on an area reaching from the electrode (14,16) to a top of the resin layer 20 (paragraph [0081]);

wherein the electrode (14,16) has a first rim part facing a periphery of the semiconductor substrate 10 and a second rim part facing a center region of the semiconductor substrate 10 (see Fig. 2 labeled by the examiner below), and

wherein the resin layer 20 is formed so as to overlap the second rim part, leaving out an area from the periphery of the semiconductor substrate 10 to the first rim part of the electrode (14,16).

FIG. 2



Regarding claim 2, Yamaguchi (Fig. 2) discloses that a passivation film 18 having an opening which exposes a part of the electrode (14,16) is formed on the side of the semiconductor substrate 10 where the electrode is formed, and the resin layer 20 is formed on the passivation film 18 (paragraph [0079]).

Regarding claim 3, Yamaguchi discloses that the resin layer 20 is formed leaving out the exposed part by the opening of the electrode (14,16) (paragraph [0080]).

Regarding claim 4, Yamaguchi (Fig. 2) discloses that a center of the opening is positioned so as to deviate from a center of the electrode (14,16) towards the periphery of the semiconductor substrate 10.

Regarding claim 5, Yamaguchi (Fig. 13) discloses a circuit board 1000 on which a semiconductor device 1 that described in the above is mounted (paragraphs [0068] and [0103]).

Regarding claim 6, Yamaguchi (Figs. 14-15) discloses an electronic equipment having the above semiconductor device (paragraph [0069]).

Regarding claim 11, Yamaguchi (Fig. 2) discloses a semiconductor device, comprising:

means for accommodating an integrated circuit 12 (paragraph [0077]) and an electrode (14,16) (paragraph [0078]);

a resin layer 20 provided on a side of the means for accommodating where the electrode is formed (paragraph [0080]); and

a wiring layer 22 formed on an area reaching from the electrode (14,16) to a top of the resin layer 20 (paragraph [0081]);

wherein the electrode (14,16) has a first rim part facing a periphery of the means for accommodating and a second rim part facing a center region of the means for accommodating (see Fig. 2), and

wherein the resin layer 20 is formed so as to overlap the second rim part, leaving out an area from the periphery of the means for accommodating to the first rim part of the electrode (14,16).

Regarding claims 12-13, Yamaguchi discloses further comprising a plurality of external terminals 24 electrically connected to the wiring layer 22 (paragraph [0082], lines 1-3).

Regarding claims 15-16, Yamaguchi discloses further comprising a resist layer 30 covering a part of the wiring layer 22 (paragraph [0086], lines 1-6).

Regarding claims 18-19, Yamaguchi discloses further comprising a coat layer (a third resin layer, not shown) formed on the resist layer 30 (paragraph [0091], lines 1-5).

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 and 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Nagai et al. (U.S Pat. 6,396,145).

Regarding claim 1, Nagai (Figs. 2a-2f) discloses a semiconductor device, comprising:

a semiconductor substrate 1 (column 11, lines 11-15 and column 3, lines 34-37) including an integrated circuit (not shown, see column 11, lines 11-15) and an electrode 2 (column 11, lines 22-24);

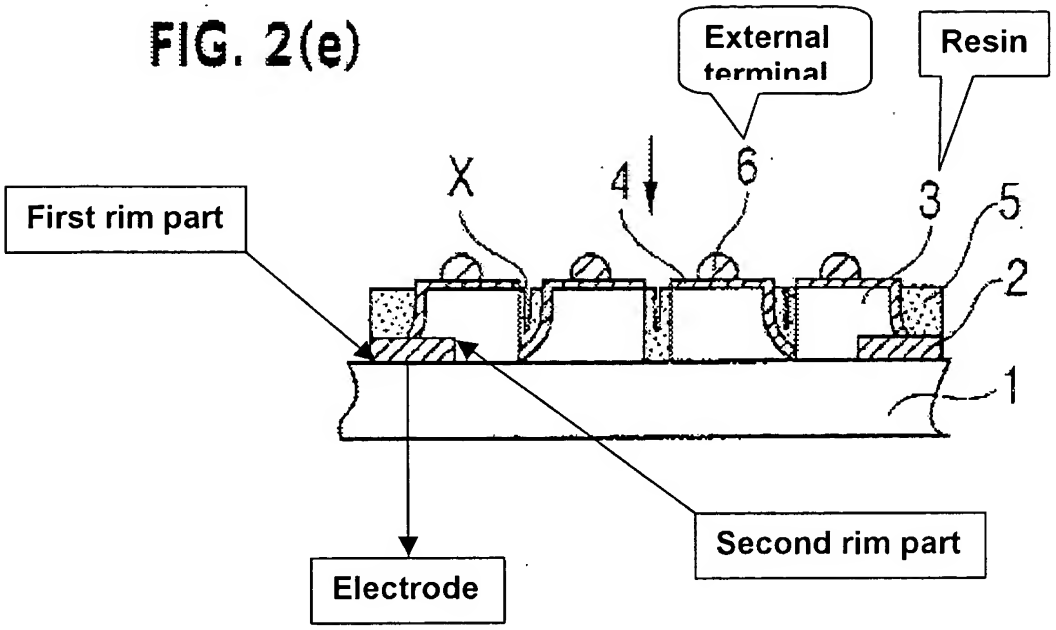
a resin layer 3 (column 11, lines 25-28 and column 7, lines 63-67) provided on a side of the semiconductor substrate 1 where the electrode 2 is formed; and

a wiring layer 4 formed on an area reaching from the electrode 2 to a top of the resin layer 3 (Fig. 2b and column 11, lines 36-43);

wherein the electrode 2 has a first rim part facing a periphery of the semiconductor substrate 1 and a second rim part facing a center region of the semiconductor substrate (see Fig. 2e labeled by the examiner below), and

wherein the resin layer 3 is formed so as to overlap the second rim part, leaving out an area from the periphery of the semiconductor substrate to the first rim part of the electrode 2 (see Fig. 2e and Fig. 4).

FIG. 2(e)



Regarding claim 11, Nagai (Figs. 2a-2f) discloses a semiconductor device, comprising:

means for accommodating an integrated circuit (not shown, see column 11, lines 11-15) and an electrode 2 (Fig. 2a and column 11, lines 22-24);

a resin layer 3 (column 11, lines 25-28 and column 7, lines 63-67) provided on a side of the means for accommodating where the electrode 2 is formed; and

a wiring layer 4 formed on an area reaching from the electrode 2 to a top of the resin layer 3 (Fig. 2b and column 11, lines 36-43);

wherein the electrode 2 has a first rim part facing a periphery of the means for accommodating and a second rim part facing a center region of the means for accommodating (see Fig. 2e); and

wherein the resin layer 3 is formed so as to overlap the second rim part, leaving out an area from the periphery of the means for accommodating to the first rim part of the electrode 2 (Fig. 2e and Fig. 4).

Regarding claims 12-13, Nagai further discloses a plurality of external terminals 6 electrically connected to the wiring layer 4 (column 11, lines 55-59).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday to Friday from 7:00AM - 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Theresa Doan T Doan
July 7, 2005.